a via coupling the first conductive layer portion to the substrate.

119. (previously presented) The method of claim 118, wherein the via is a redundant via.

120. (previously presented) The method of claim 118, wherein the test structure further comprises a plurality of stacked conductive layers and vias to form a multilevel test structure.

121. (previously presented) The method of claim 120, wherein at least one of the vias is a redundant via.

REMARKS

Claim 108 has been amended merely to clarify the invention. Claims 108-121 remain pending.

The Examiner rejected claims 108, 109 and 114-117 under 35 U.S.C. U.S.C. §103(a) as being unpatentable over Satya et al. (US 5,959,459) in view of Chiang et al. (US 6,309,956). Additionally, claims 110, 112, 113, 118, and 120 are rejected under 35 U.S.C. §103(a) as being unpatentable over Satya et al. in view of Chiang et al., and further in view of Huang et al. (US 6,001,733). Claims 111, 119, and 120 are rejected under 35 U.S.C. §103(a) as being unpatentable over Satya et al. and Chiang et al. in view of Huang et al., and further in view of Bennett (US 3,861,023). The Examiner's rejections are respectfully traversed as follows.

Claim 108 is directed towards a "method of fabricating a semiconductor die." Claim 1 also requires "forming a test structure on the semiconductor die, wherein at least a portion of the test structure includes a dummy structure in a top conductive layer, wherein the test structure permits voltage contrast testing" and "performing voltage contrast testing on the test structure to detect electrical defects within the test structure." In other words, voltage contrast testing is performed on a test structure which includes a dummy structure in a top conductive layer.

The Satya et al. reference is directed towards test structures and methods of performing voltage contrast testing on such test structures. However, the Satya et al. reference fails to teach that the voltage contrast test structure includes a dummy structure, in the manner claimed. It is also respectfully submitted that the secondary reference Chiang et al. also fails to teach or suggest a test structure having a dummy structure which can be combined with the voltage

contrast structures of the Satya reference to thereby result in the claimed voltage contrast structure.

The Chiang et al. reference generally teaches how dummy structures can be used along with a low k dielectric to result in a more stable interconnect structure. For example, Chiang et al. teaches that the placement of dummy structures and a low k dielectric material surrounding the dummy structures in a particular metal layer results in a reduced capacitance between the metal lines of the metal layer. See Col. 5, Lines 41-48. Throughout the disclosure, Chiang et al. only teaches embodiment which include dummy structures in a metal layer which are completely covered with a low k dielectric. See, for example, Figures 4 and 5 and Col. 4, lines 48-52. Chiang et al. clearly teaches that the dummy structures *must* be covered by such a dielectric (as well as other metal layers in certain embodiments) so as to achieve the goal of providing a more stable interconnect structure. At col. 4, lines 54-59, Chiang et al. teaches "It should be noted in one embodiment dummy structure 412 is not electrically connected to any other conductor and in the illustrated embodiment is surrounded on all sides except the bottom by the low k dielectric material typically organic polymer." Even when the dummy structures are provided in an upper metal layer, they are still surrounded by the low k dielectric: "A dummy structure in layer 432 would be completely encased on all sides by low k dielectric." See Col. 4, Lines 62-66.

Since the dummy structures of Chiang et al. are always surrounded by a low k dielectric material, Chiang et al. teaches away from the present invention. That is, one would not be able to perform a voltage contrast test on the dummy structures of Chiang et al. since they are taught as being always surrounded by a low k dielectric material. Accordingly, one would not be motivated to combine the dummy structures of Chiang et al. with voltage contrast test structure since Chiang et al. teaches away from dummy structures which can also form a part of a voltage contrast test structure. In other words, the dielectric material which surrounds the dummy structures of Chiang et al. would prevent one from directing an electron beam at the dummy structures for a voltage contrast test. Accordingly, one would not be motivated to combine the dummy structures of Chiang et al. which can not be used with a voltage contrast test with the voltage contrast test structures of Satya et al.

Although amendment of claim 108 is not necessary to overcome the Examiner's rejections, claim 108 has been amended to clarify that the dummy structure is in the top conductive structure. Such a limitation is also inherent in the claim language which requires that the test structure permit voltage contrast testing. That is, a voltage contrast test can only be performed on a top conductive layer (although it can also be coupled to underlying layers). The cited references also fail to teach a test structure having a dummy structure which is in the top conductive layer, in the manner claimed.

telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Mary Olynick
Reg. 42,963

P.O. Box 778
Berkeley, CA 94704-0778
(510) 843-6200